

What is claimed is:

1. A method of designing an integrated circuit, comprising:
 - identifying a programmable logic core;
 - identifying an application;
 - designing an application specific circuit for the application;

and

integrating the programmable logic core into the designed application specific circuit.

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2. A method of designing an integrated circuit, comprising:

identifying a programmable logic core for the integrated circuit;

establishing a set of timing constraints associated with the programmable logic core; and

controlling the design of application specific circuit that interfaces with the programmable logic core in the integrated circuit in accordance with the set of timing constraints.

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3. A method of designing an integrated circuit, comprising:

identifying a programmable logic core for the integrated circuit;

establishing a sign-off design associated with the programmable logic core; and controlling the design of application specific circuit that interfaces with the programmable logic core in the integrated circuit in accordance with the sign-off design.

4. An integrated circuit, comprising:
- a programmable logic core; and
 - application specific circuitry, the application specific circuitry being designed in accordance with a sign-off design.
- 10 5. An integrated circuit according to claim 4, wherein the programmable logic core includes:
- a programmable multi-scale array;
 - an application circuit interface for providing a signal interface between the programmable multi-scale array and the application specific circuitry; and
 - a programmable logic adapted that configures the programmable multi-scale array.